

Application No.: 10/777,599

Docket No.: JCLA12098

### AMENDMENTS

#### To the Claims:

Please amend the claims as indicated hereafter.

#### **Claims 1-3 (cancelled)**

Claim 4. (currently amended) A voltage level shifter, comprising:

an AND gate for processing a first control signal and an input signal to produce a synchronizing signal, wherein the first control signal is a periodic signal;

a transistor device having a first transistor and a second transistor, wherein a drain of the first transistor and a drain of the second transistor are electrically connected at a first contact point, a source of the first transistor then is electrically connected to a ground and a source of the second transistor is electrically connected to a voltage source, a gate of the first transistor is electrically connected to the synchronizing signal and a gate of the second transistor is electrically connected to a second control signal having the same phase as the first control signal ;

a switch, controlled by the ~~first~~ second control signal, wherein one terminal of the switch is electrically connected to the first contact point and the other terminal of the switch is electrically connected to a second contact point;

a buffer for producing an output signal, wherein an input terminal of the buffer is connected to the second contact point; and

a capacitor, wherein one terminal of the capacitor is electrically connected to the second contact point for storing a signal level of the second contact point, and the other terminal of the capacitor is electrically connected to the ground.

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Claim 5. (original) The voltage level shifter of claim 4, wherein the switch comprises an n-type metal oxide semiconductor.

**Claim 6. (cancelled)**

Claim 7. (previously presented) The voltage level shifter of claim 4, wherein the buffer comprises an inverter having at least a PMOS transistor and a NMOS transistor.

Claim 8. (previously presented) The voltage level shifter of claim 4, wherein the capacitor comprises a transistor provided as a parasitic capacitor.

**Claims 9-10 (cancelled)**

Claim 11. (previously presented) The voltage level shifter of claim 4, wherein the AND gate comprises a low voltage transistor device, and the transistor device, the buffer and the capacitor comprise high voltage transistor devices.

**Claims 12-13 (cancelled)**

Claim 14. (currently amended) A voltage level shifter, comprising:

a switch;

an input transistor device comprises:

a first transistor, electrically connected to a voltage source;

a second transistor; and

a third transistor, electrically connected to a ground;

wherein the first transistor is a PMOS transistor, the second and third transistors are NMOS transistors, a gate of the first transistor and a gate of the second transistor are electrically connected to a first control signal, a gate of the third transistor is electrically

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connected to an input signal, and a drain of the first transistor and a drain of the second transistor are electrically connected at a first contact point, and a source of the third transistor is electrically connected to a ground and a drain of the third transistor is electrically connected to a source of the second transistor;

wherein the switch is controlled by the first control signal, in which one terminal of the switch is electrically connected to the first contact point;

a capacitor, electrically connected to ~~the other~~ another terminal of the switch at a second contact point for storing a signal level of the second contact point; and

a buffer for producing an output signal, wherein the input terminal of the buffer is electrically connected to the second contact point.

Claim 15. (previously presented) The voltage level shifter of claim 14, wherein the capacitor comprises a transistor provided as parasitic capacitor .

Claim 16. (currently amended) The voltage level shifter of claim 14, ~~said capacitor~~ further comprising:

a fourth transistor;

a fifth transistor; and

a second control signal;

wherein the capacitor is electrically connected to the fourth transistor, in which a drain, a gate and a source of the fourth transistor are electrically connected to the second contact point, an output terminal of the buffer and the fifth transistor respectively, a gate of the fifth transistor is electrically connected to the second control signal, and the fourth and the fifth transistors are

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PMOS transistors.

Claim 17. (previously presented) The voltage level shifter of claim 16, wherein the first control signal is a periodic negative pulse and the second control signal is a periodic positive pulse, the first and the second control signals are synchronized and a width of the negative pulse is narrower than a width of the positive pulse.

Claim 18. (original) The voltage level shifter of claim 16, wherein the first, second, third, fourth and fifth transistors and the buffer comprise high voltage field effect transistor devices.